Test-Beam Analysis of HGTD Prototype Modules for the ATLAS Phase-II Upgrade

Karabo Tau[1],

Rachid Mazini[1], Roja Rimer[1], Thabo Lepota[1], Pau Fuste Martin[2]

[1]University of the Witwatersrand,

[2]The Barcelona Institute of Science and Technology

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Motivation: The High Luminosity LHC

From July 2026, LHC will be upgraded and in 2030, LHC will run in "High Luminosity" (HL-LHC)

- Instantaneous **luminosity** will be approximately a factor of **~5-7.5** higher than the LHC nominal values
- Average number of interactions per bunch crossing (pileup events) reaches **200**
- The increased pile-up and radiation levels require detector upgrades capable of maintaining excellent tracking and timing performance in the forward region .

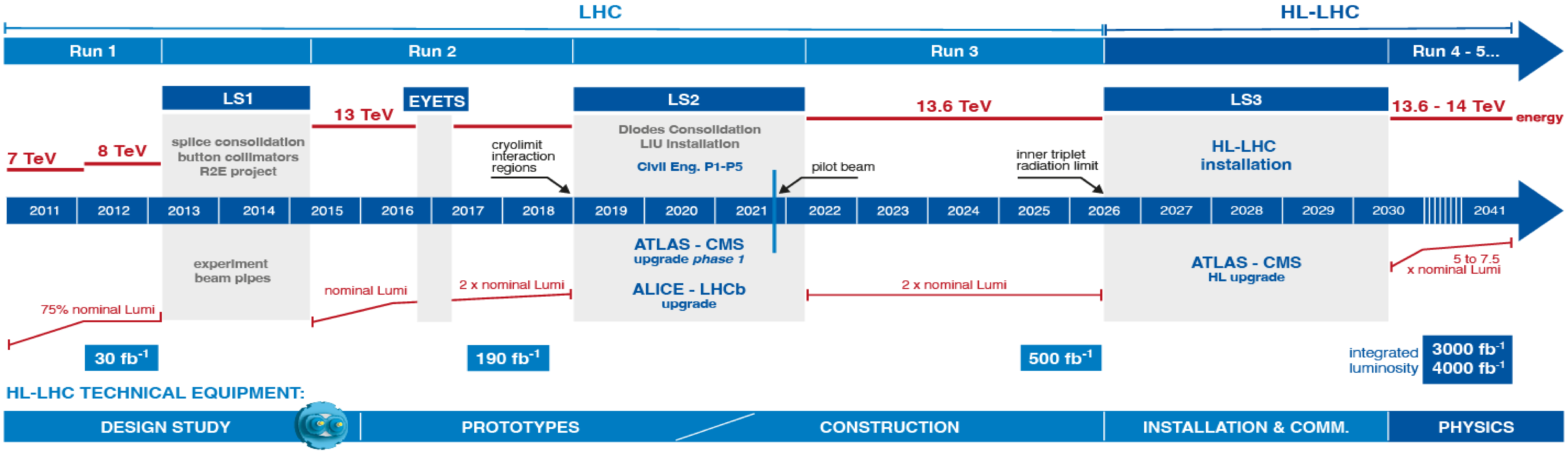


Figure 1: LHC/ HL-LHC Plan

Introduction: The High Granularity Timing Detector (HGTD)

- Dedicated **timing detector** for the forward region
- **Double-sided disks** between the new Inner Tracker (ITk) end-cap rings and the end-cap calorimeters
  - Location: $\pm$ 3.5m from the interaction point
  - Coverage: 120 mm < r < 640 mm & 2.4 <|η|< 4.0
- The HGTD comprises **8032** modules
- Each HGTD module consists of LGAD sensors read out by ALTIROC ASICs
- Target time resolution:
  ~ **30 (50) ps per track beginning (end)** of HGTD lifetime
- Provide **bunch by bunch** luminosity measurements

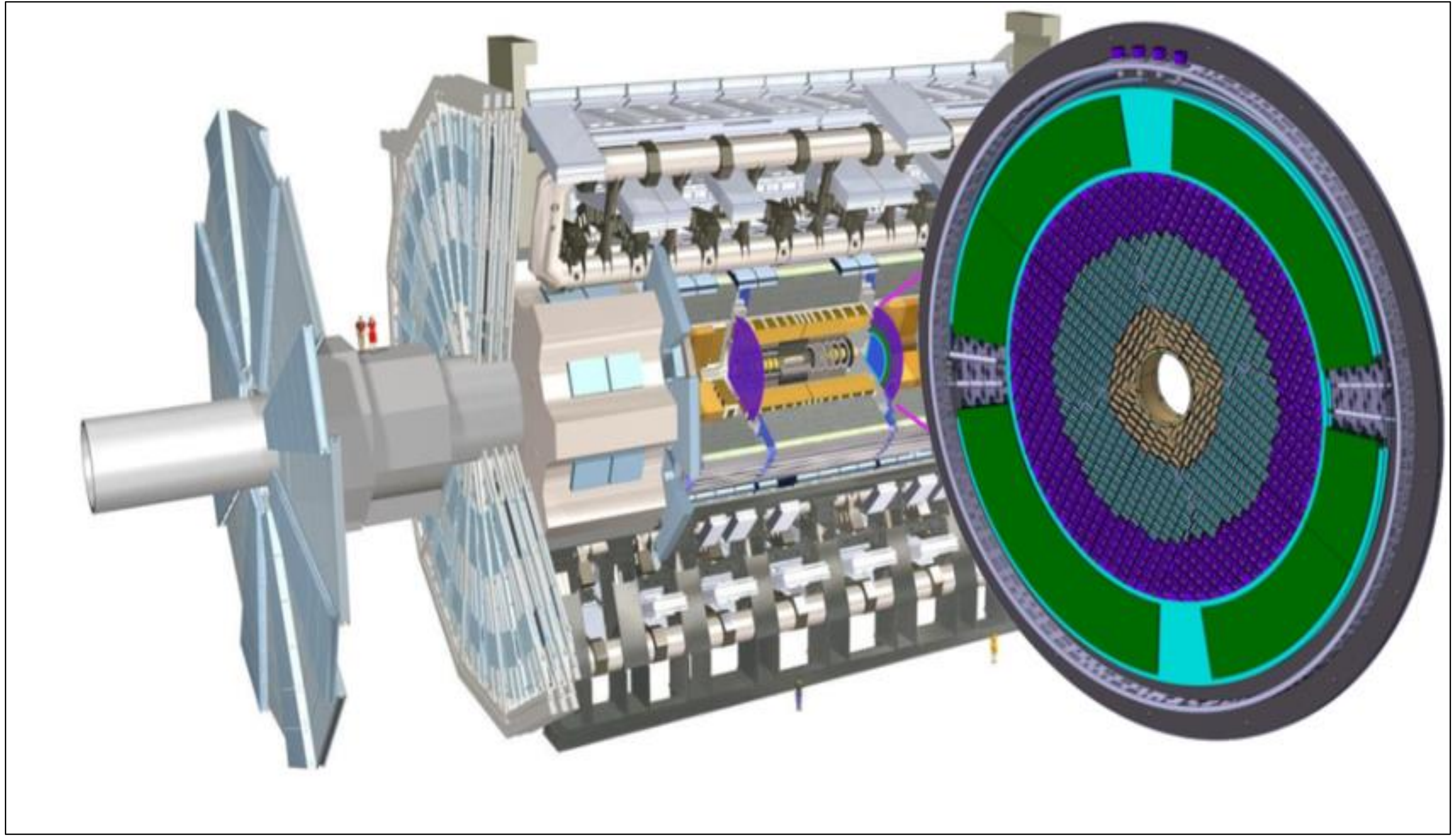


Figure 2: Position of the HGTD within the ATLAS Detector

Introduction: The HGTD LGAD sensor

Why *LGADs?*

- n-on-p structure with additional p-type gain layer
- Low gain (~10) for fast signal rise time and enhanced signal-to-noise ratio
- Fine segmentation (15 × 15 pads, 1.3 mm^2 per pad)
- Carbon-enriched gain layer for radiation hardness

HGTD Performance Targets:

- Collected charge: > **10 (4) fC per MIP** before irradiation (after irradiation)
- Hit efficiency: > **97% (>95%)** at the beginning of detector operation (end of detector lifetime)

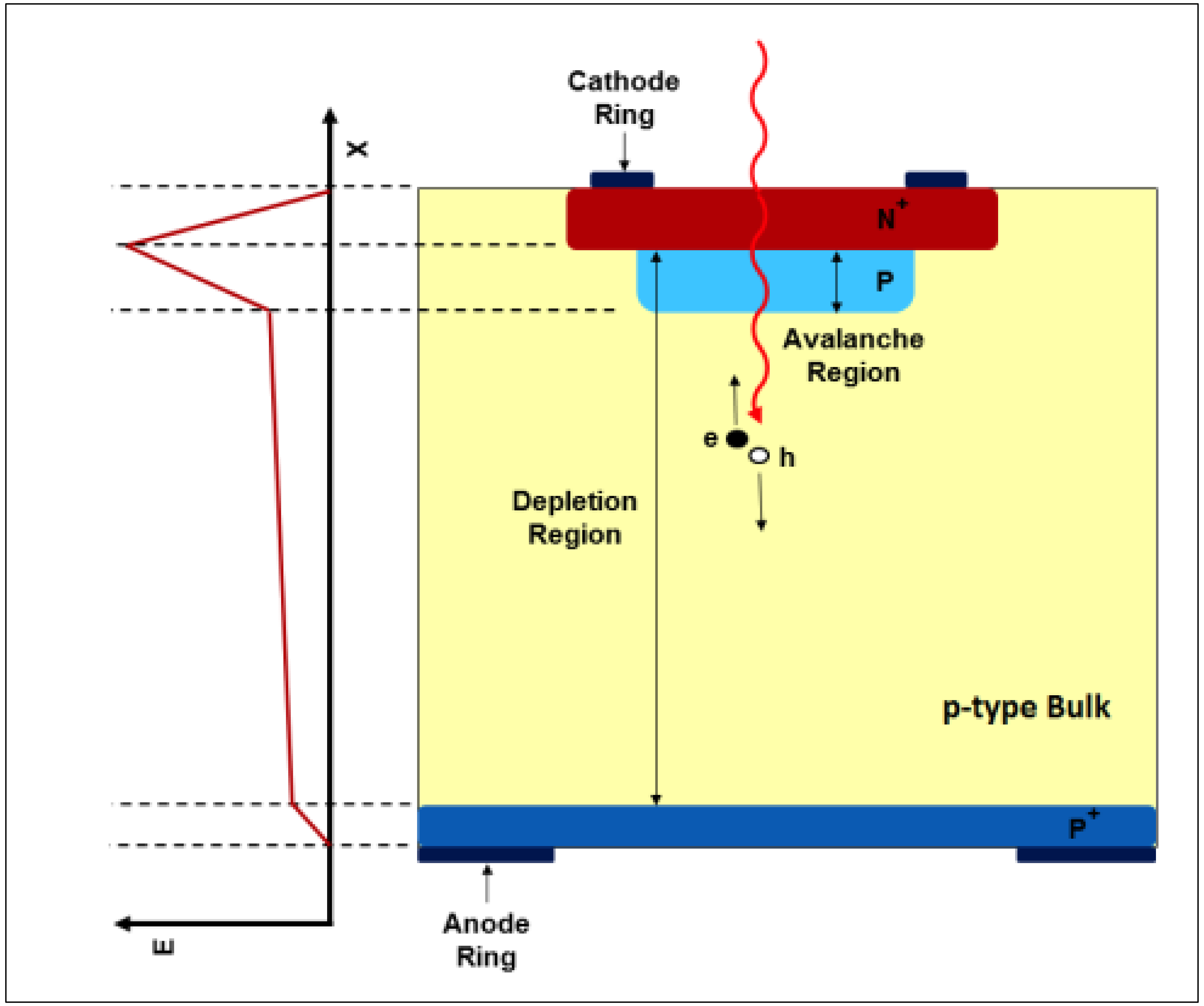


Figure 3: Cross section of an LGAD sensor

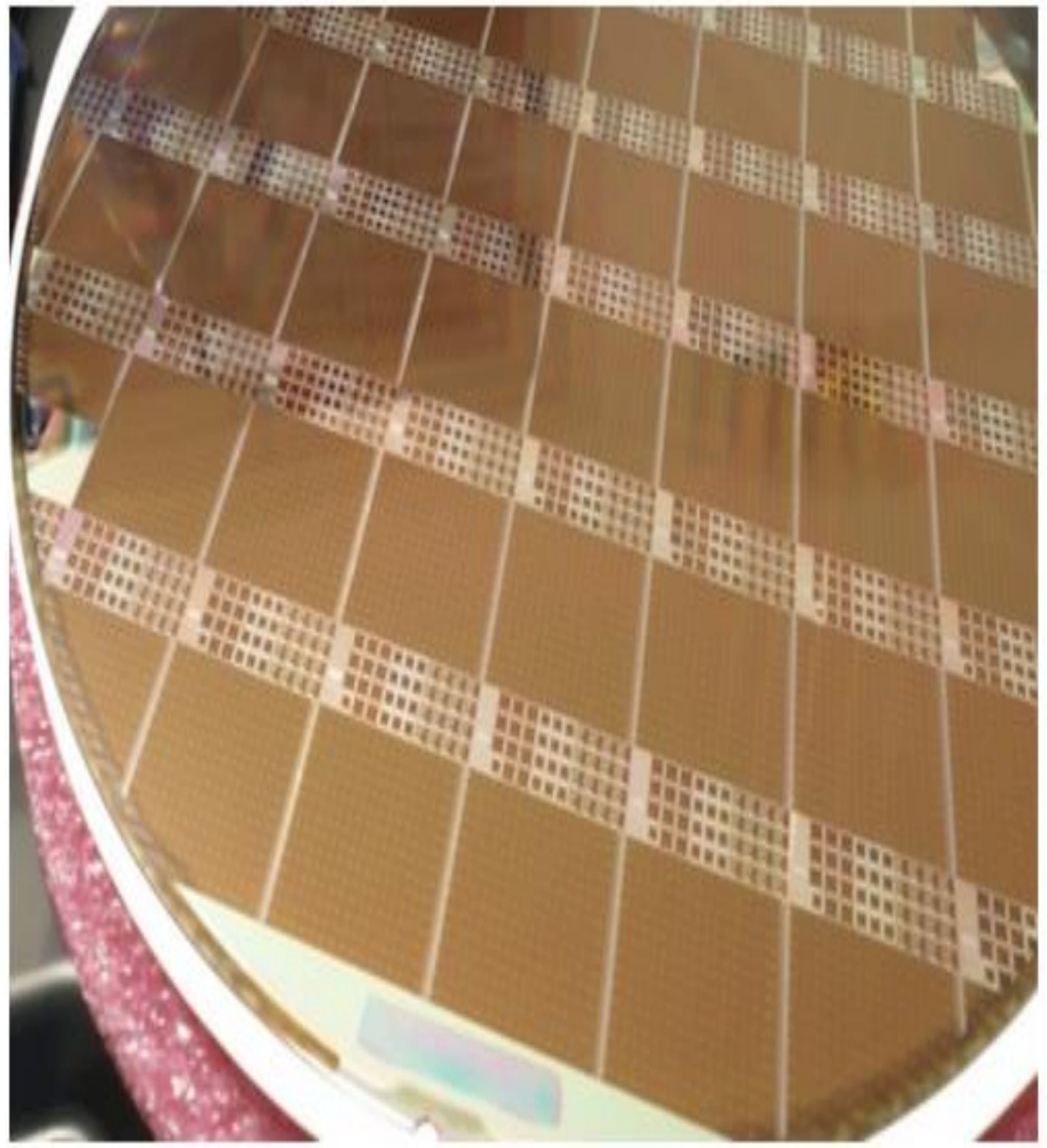
Introduction: HGTD Front-End ASIC (ALTIROC)

- **ALTIROC** (ATLAS LGAD Timing Read-Out Chips) are ASIC (Application-Specific Integrated Circuit) chips
- Designed to interface with the HGTD LGAD sensors
- **130nm** CMOS technology from TSMC
- **225** channels arranged in a **15×15** matrix

Provided measurements:

- **Time-of-Arrival** (ToA)
- **Time-over-Threshold** (ToT)

FINAL VERSION: ALTIROC-A



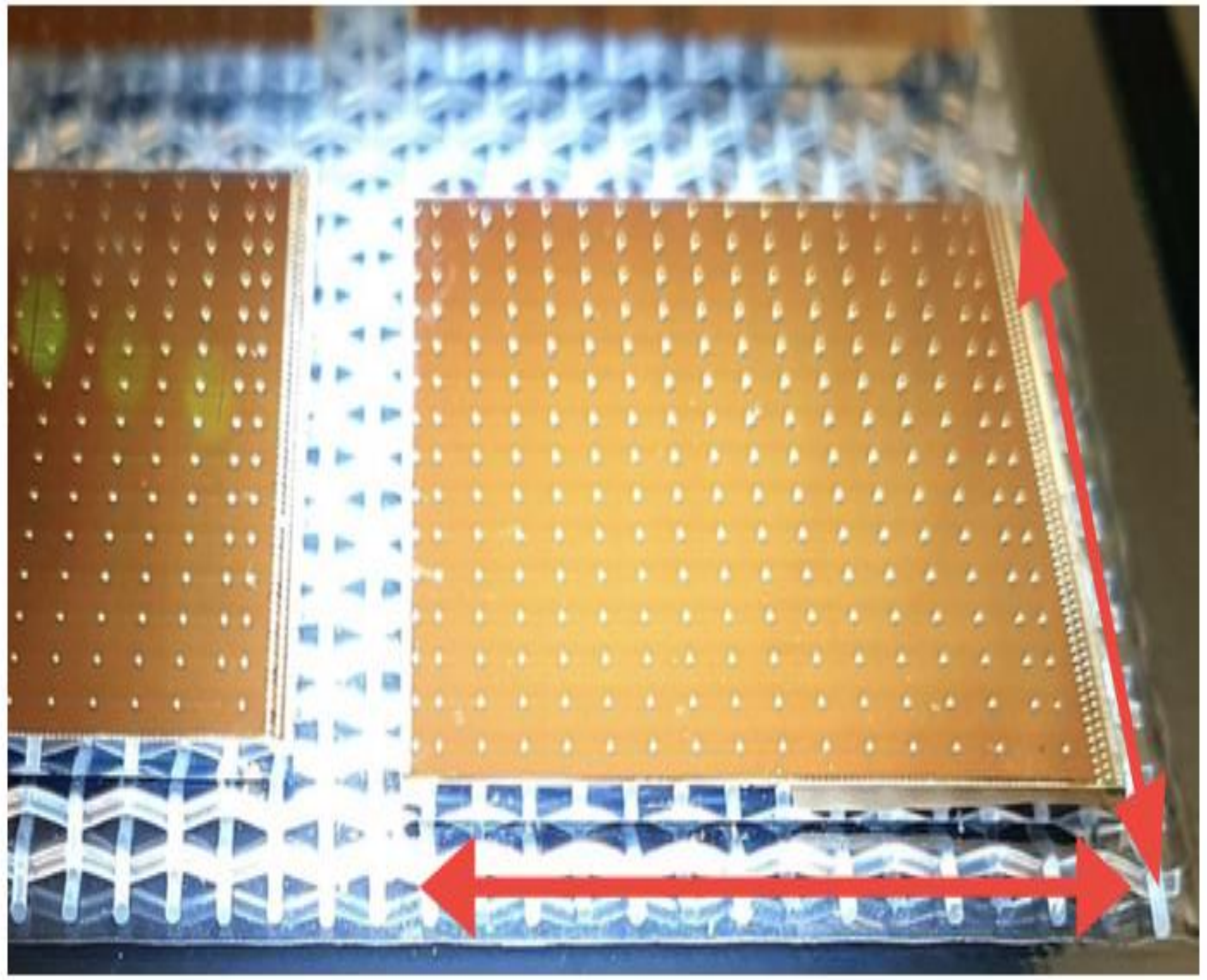


Figure 4: HGTD Front-End ASIC Chip: ALTIROC

S. Grinstein, TREDI 2025

Timing in HGTD

Contributions to Timing Resolution

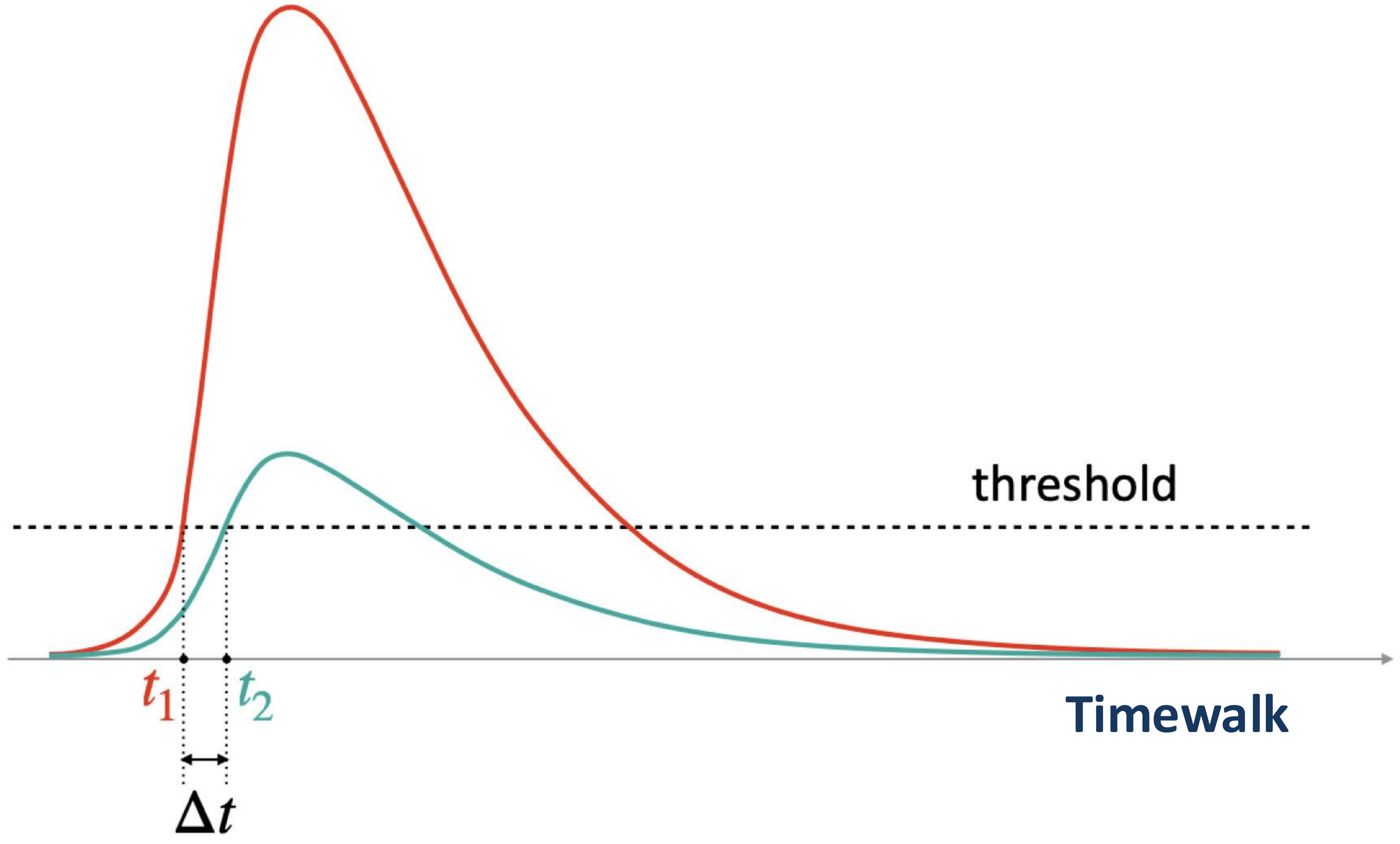
$$\sigma^2_{Total} = \boxed{\sigma^2_{Landau}} + \boxed{\sigma^2_{Timewalk} + \sigma^2_{Jitter} + \sigma^2_{Clock} + \sigma^2_{TDC}}$$

SENSOR ELECTRONICS

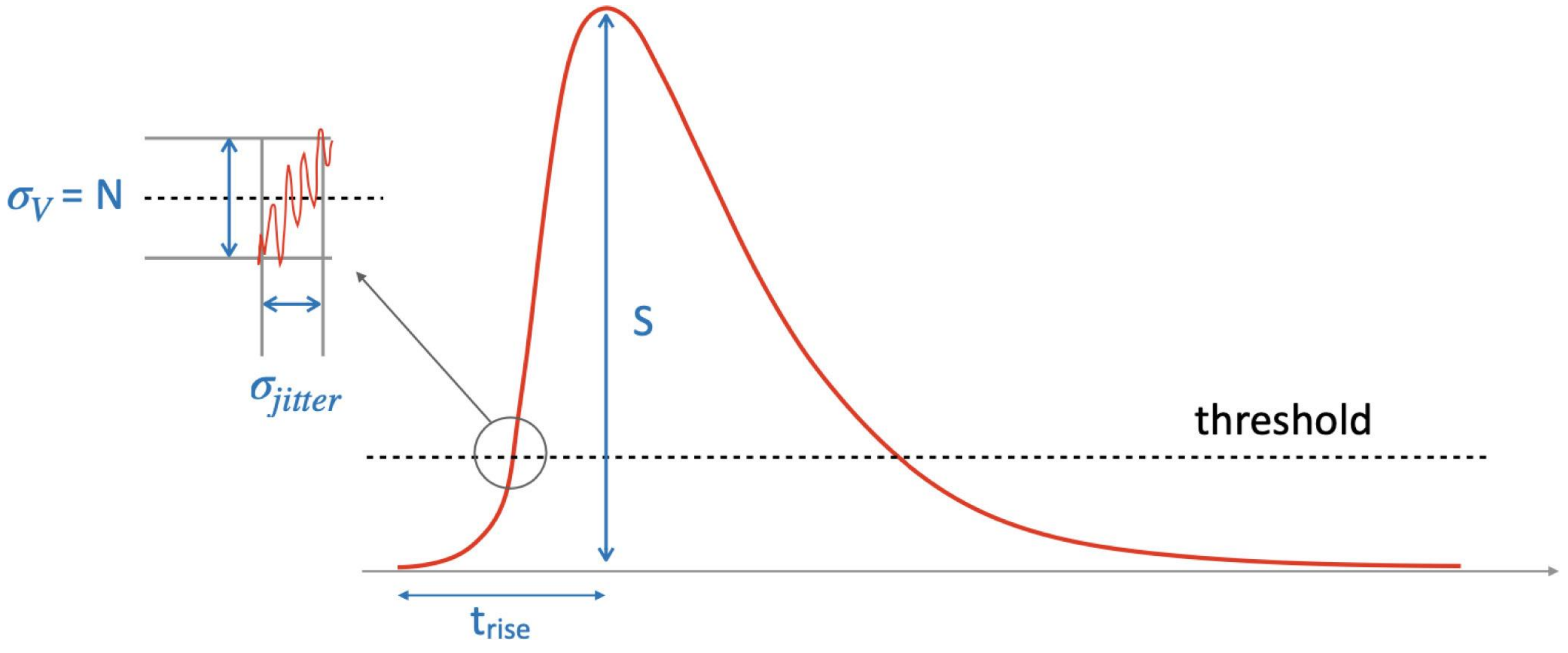
- **Landau distribution**: non-uniform energy deposition by MIPs
  - Mitigated by thin active sensor thickness
  - $\sigma_{\text{Landau}} \sim 30$ ps

- **Time-walk:** ToA dependency on signal amplitude
  - Corrected using ToT information
  - $\sigma_{\text{Time-walk}} = \frac{V_{th}}{Signal/t_{rise}}|RMS$

- **Electronic jitter:** electronic noise in the signal amplitude
- $\sigma_{\text{Jitter}} = \frac{t_{rise}}{Signal/Noise} \sim 25$ ps



Timewalk



Electronic jitter

https://doi.org/10.1016/j.physrep.2025.10.006

Experimental setup: HGTD test-beam campaigns

- HGTD modules are characterised through two complementary test-beam campaigns
- The results presented in this work are obtained from the October 2025 CERN SPS test-beam campaign

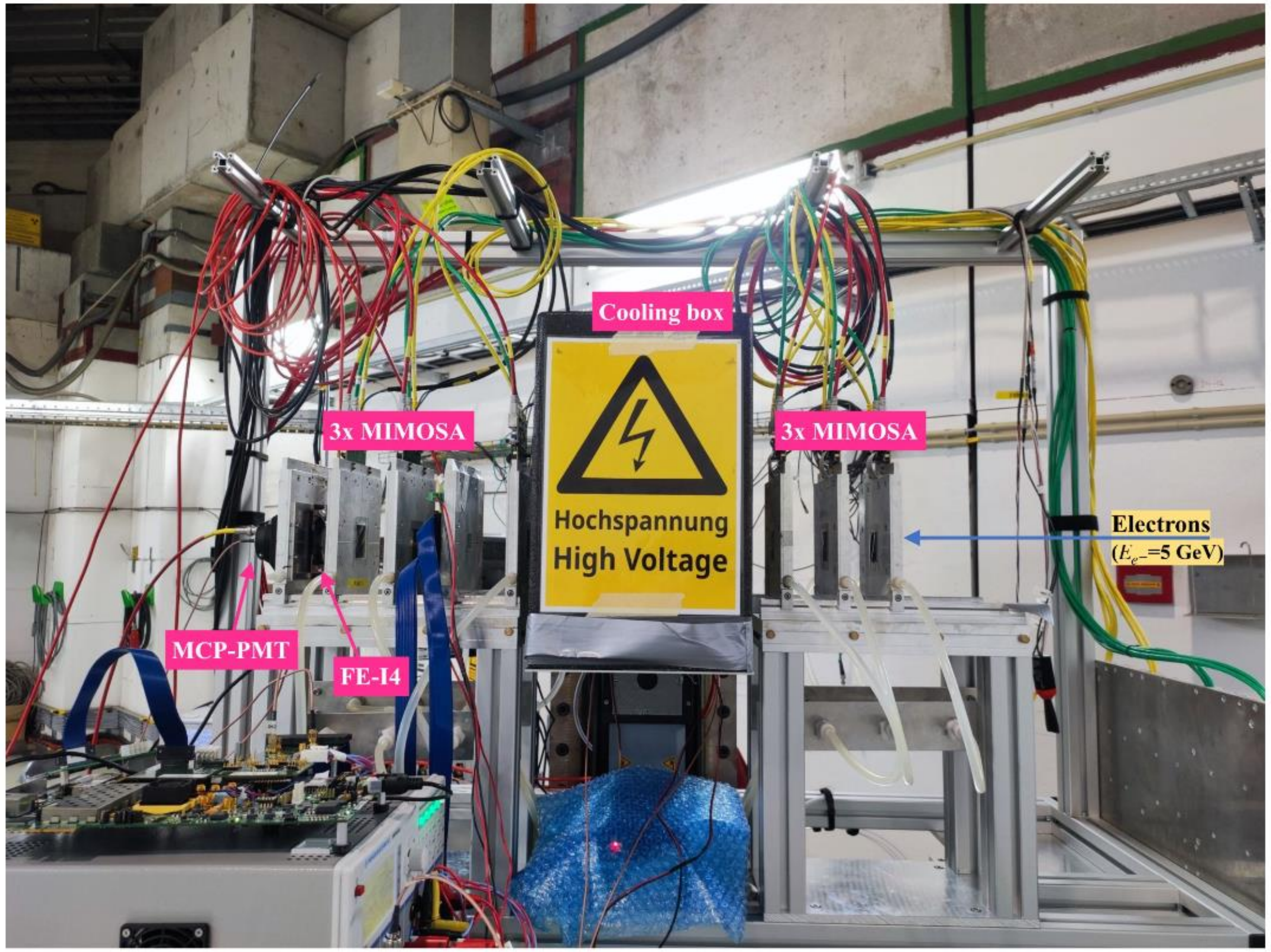


Figure 5: Test-beam setup at DESY (Germany)

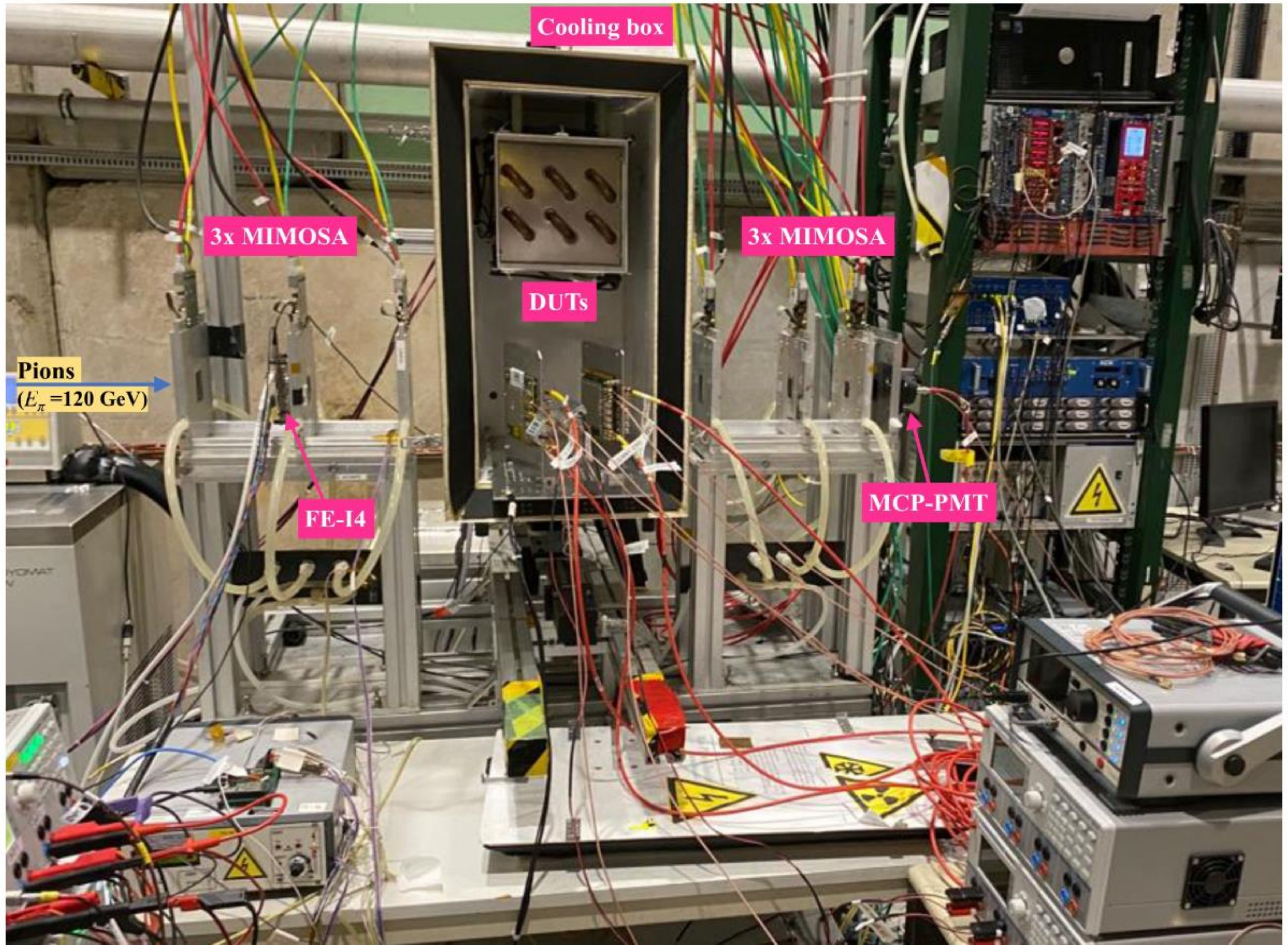


Figure 6: Test-beam setup at SPS CERN

Experimental setup: Test-beam workflow

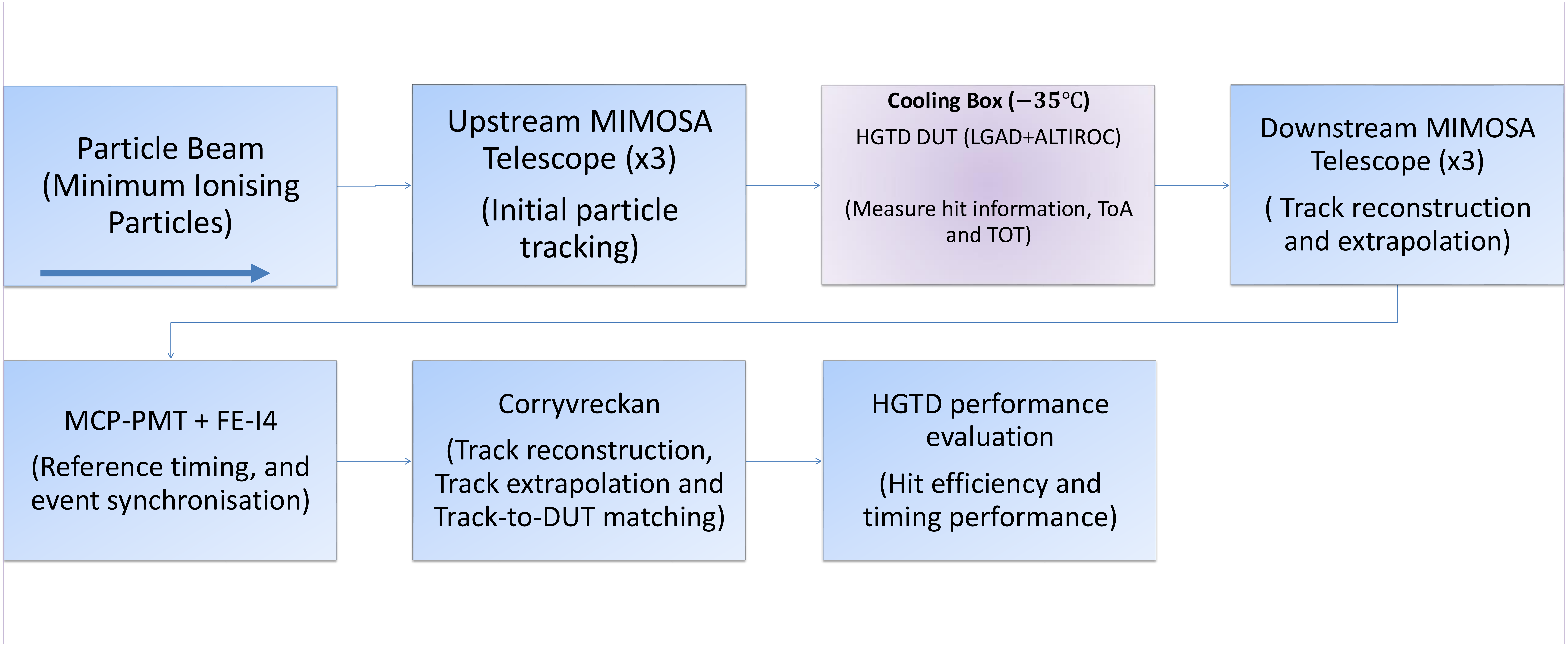


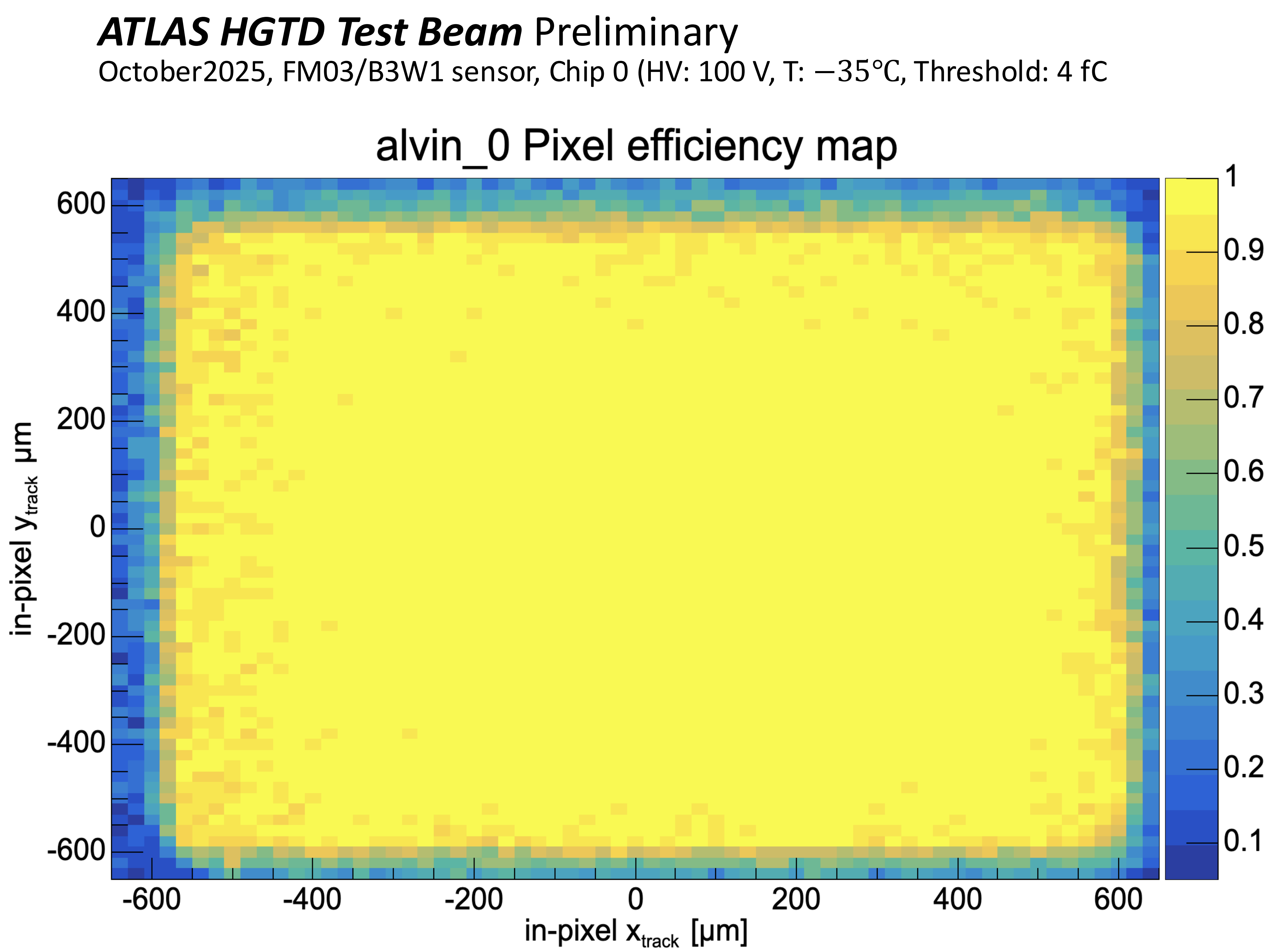
Figure 7: Schematic overview of the CERN SPS HGTD test-beam workflow

Test-beam measurements

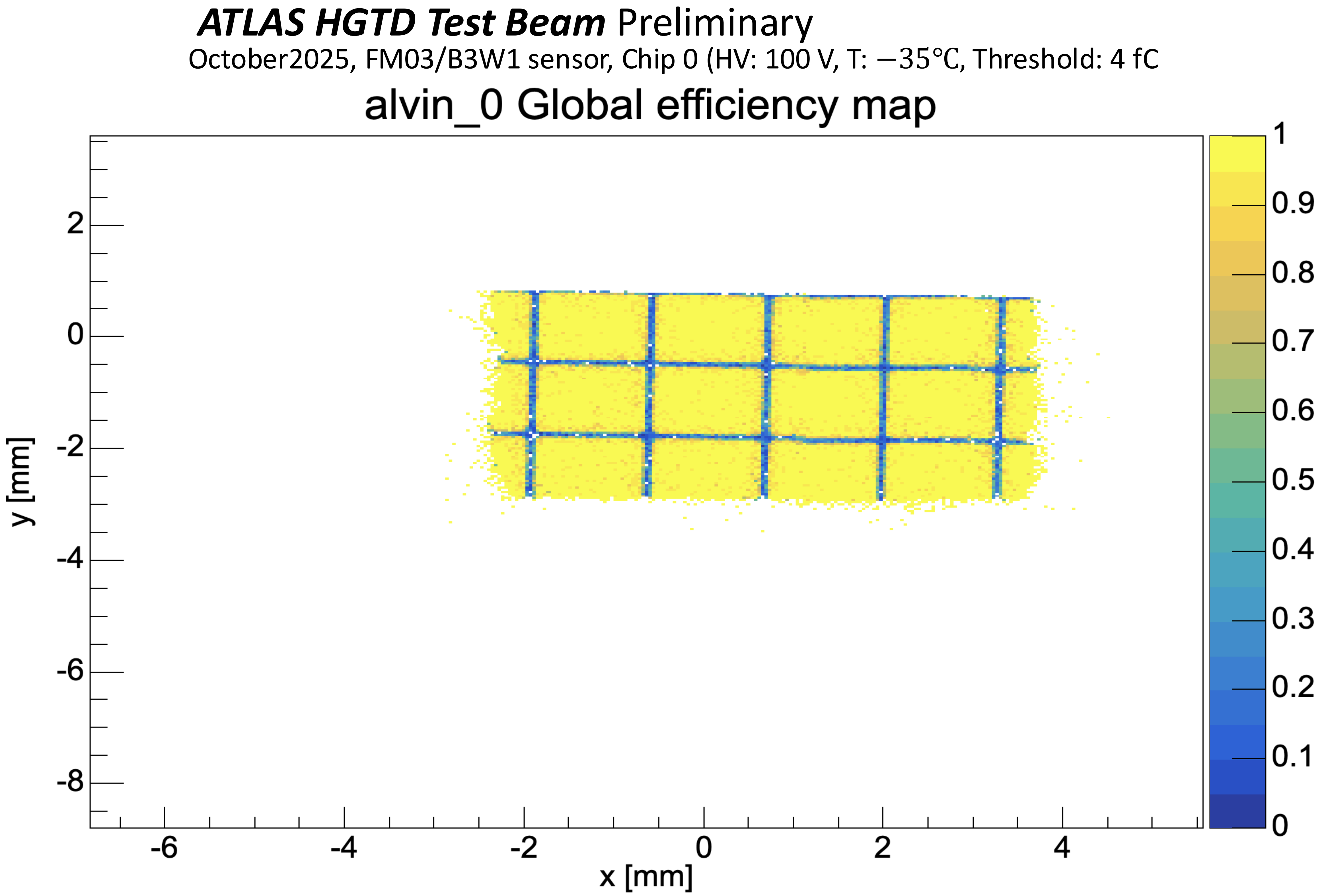
Hit Efficiency

Test-beam measurements with Alvin on ALTIROC-A modules at CERN SPS

- ☐ Batch **217**:
  - Highly uniform detector response across the active pixel
  - 98% in the gain region, exceeding HGTD design target



a) In-pixel efficiency map

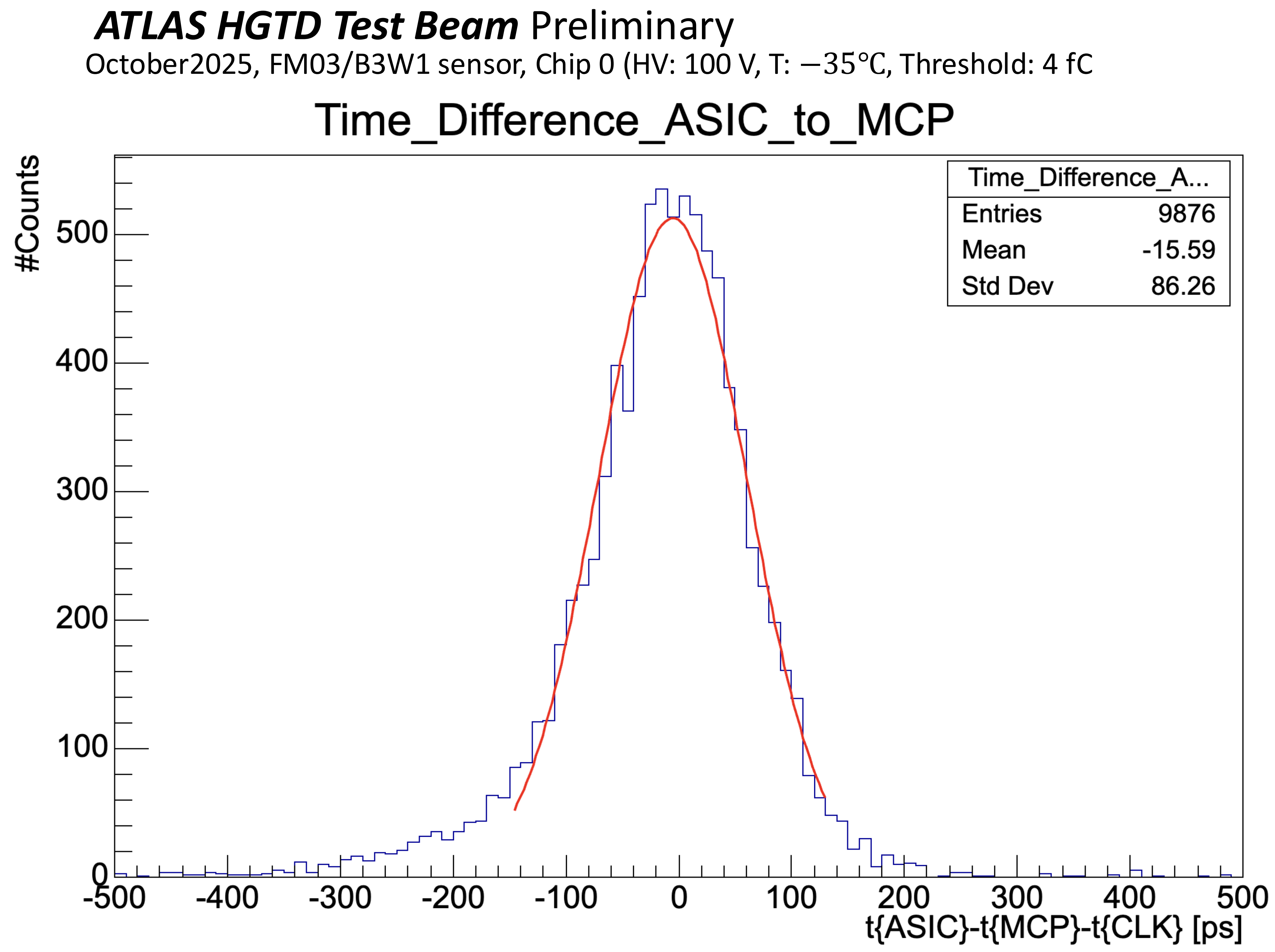


b) Global efficiency map

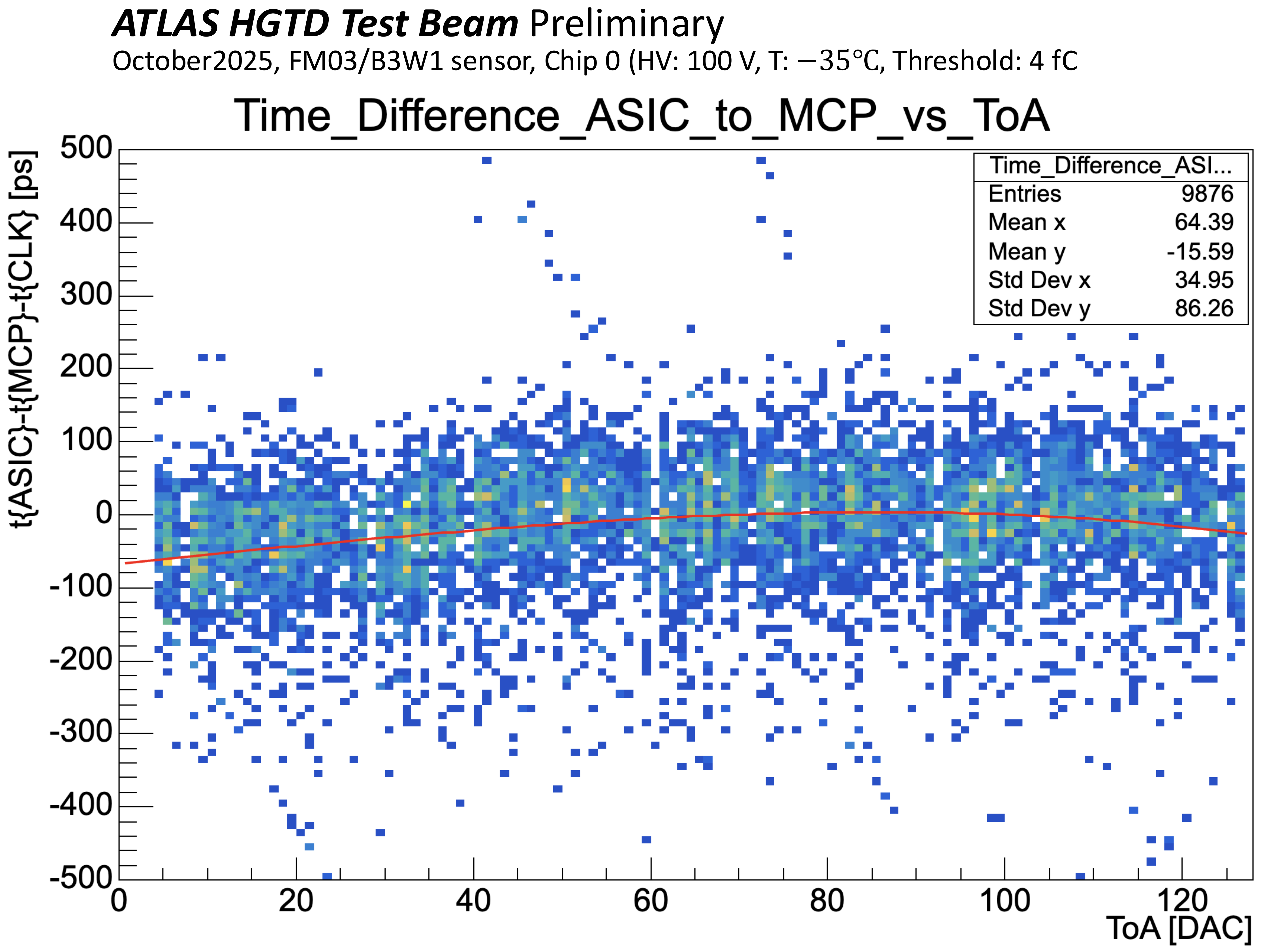
Test-beam measurements

Timing Performance

- Module tuned at threshold 4 fC and with bias voltage from 90 V to 100 V
  - Measurement performed at -35°C
  - Results shown after time-walk corrections



a) The corrected time difference between the DUT and the MCP-PMT reference detector

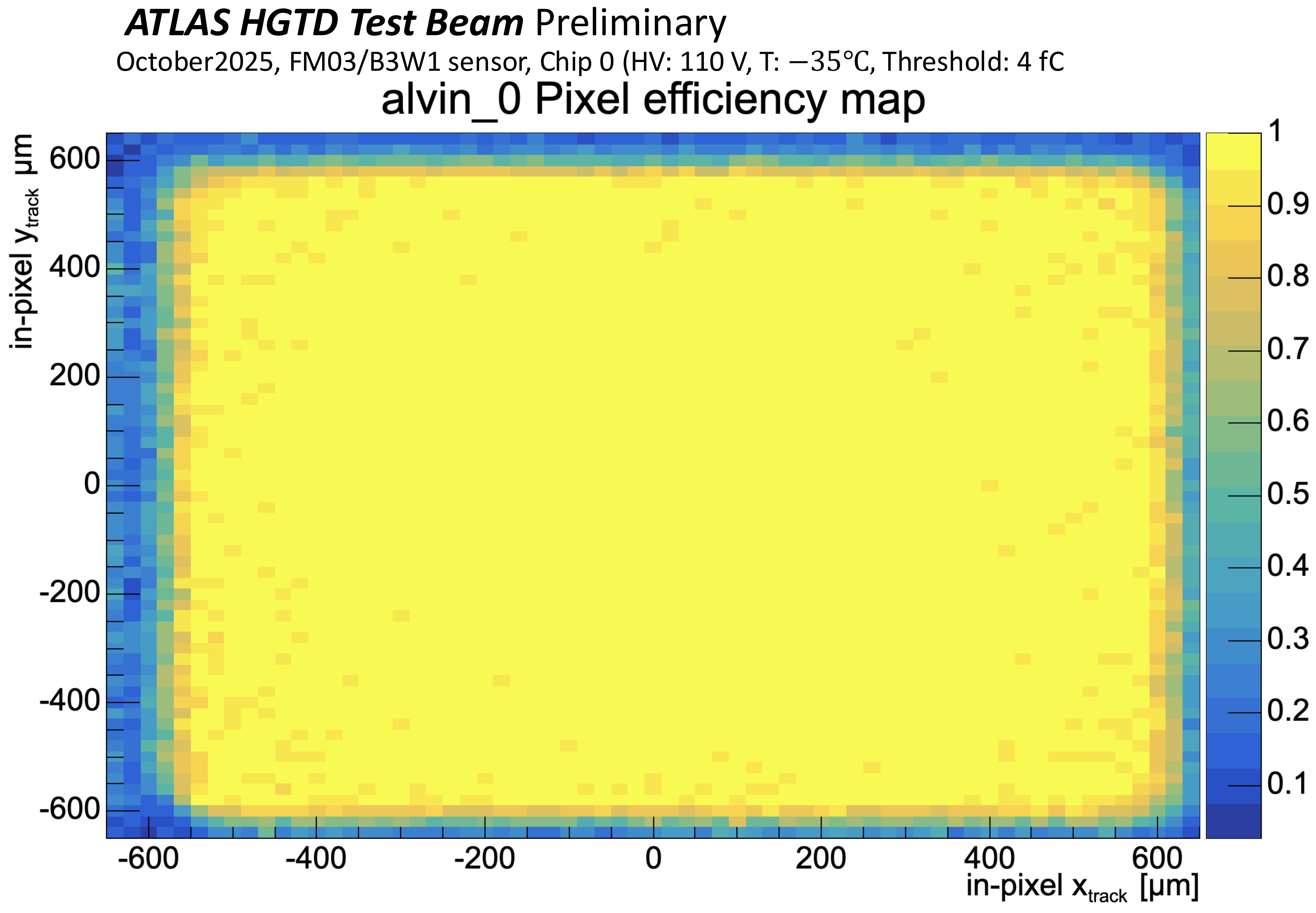


b) Residual Time Difference vs ToA

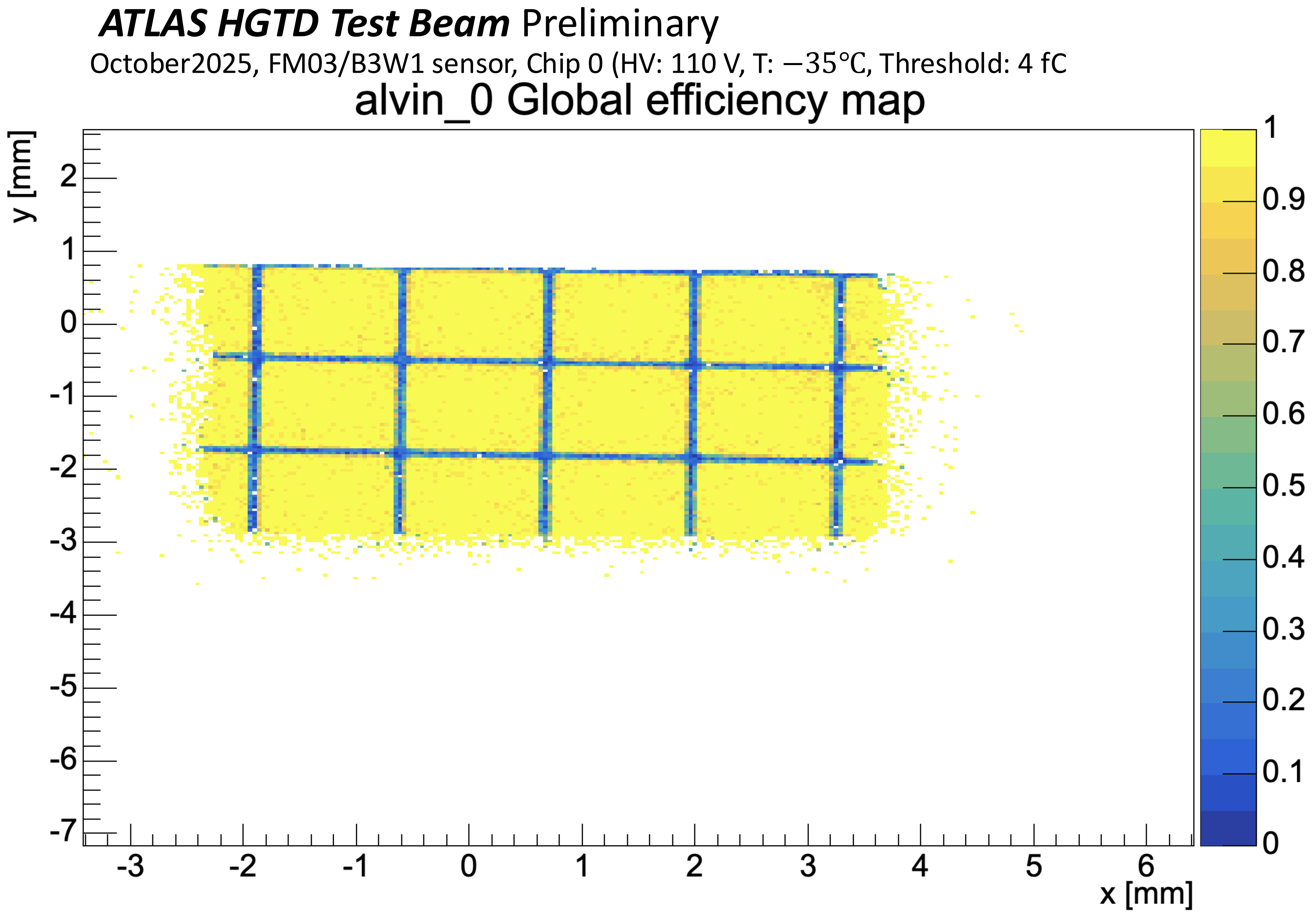
Hit Efficiency

Test-beam measurements with Alvin on ALTIROC-A modules at CERN SPS

- ☐ Batch **218**:



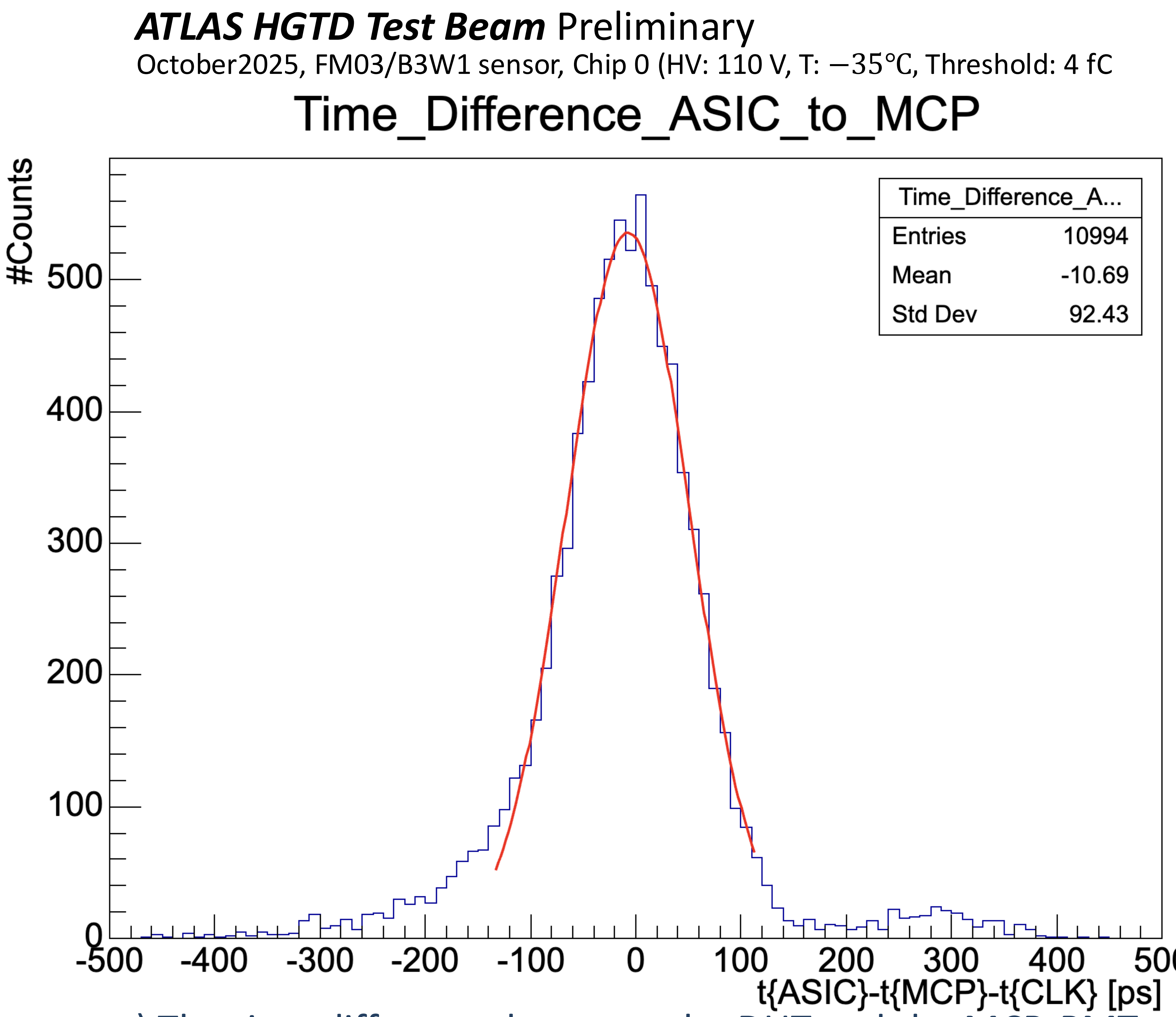
a) In-pixel efficiency map



b) Global efficiency map

Test-beam measurements

- Module tuned at threshold 4 fC and with bias voltage from 90 V to 100 V
- Measurement performed at -35ºC
- Results shown after time-walk and MCP corrections



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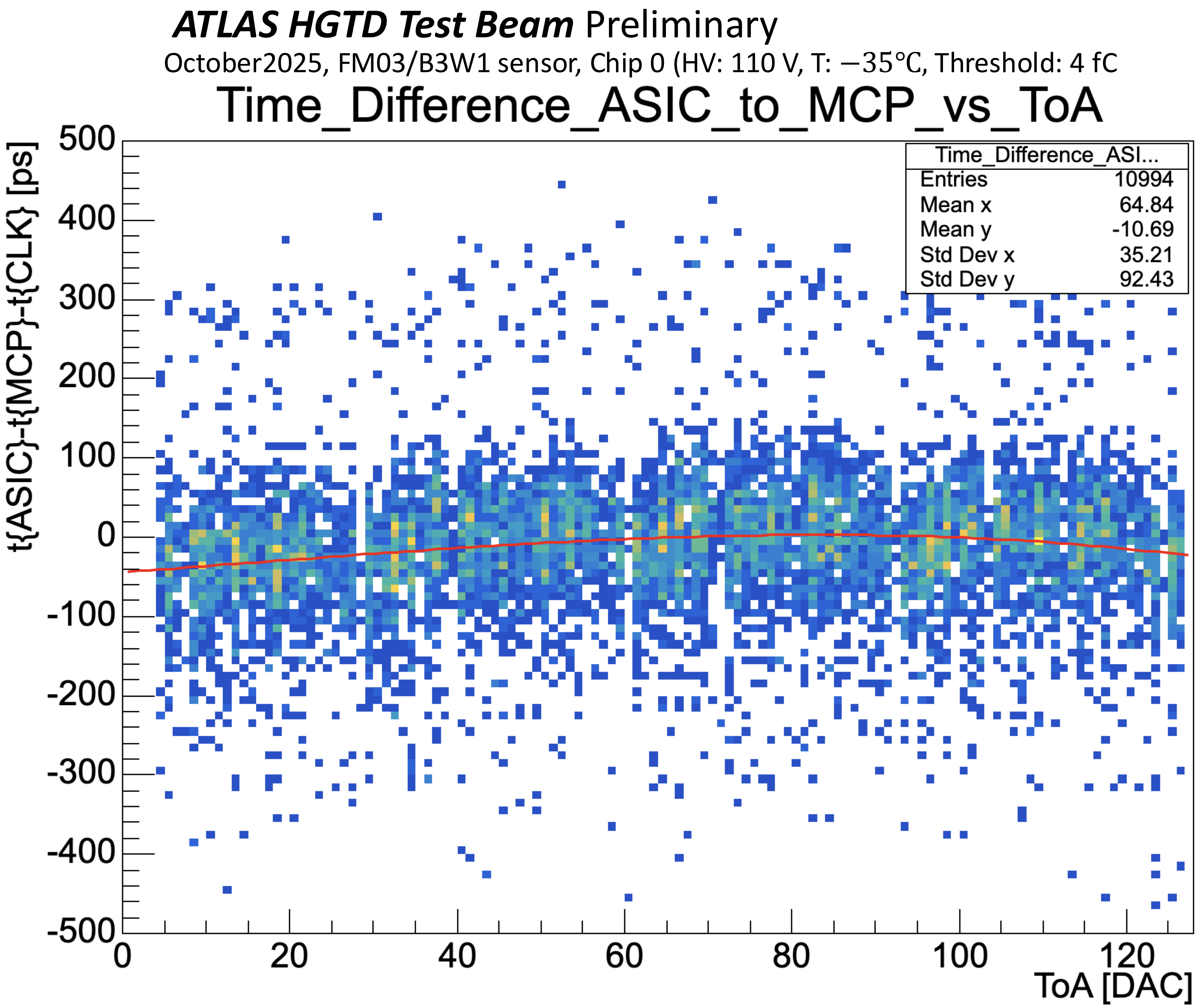
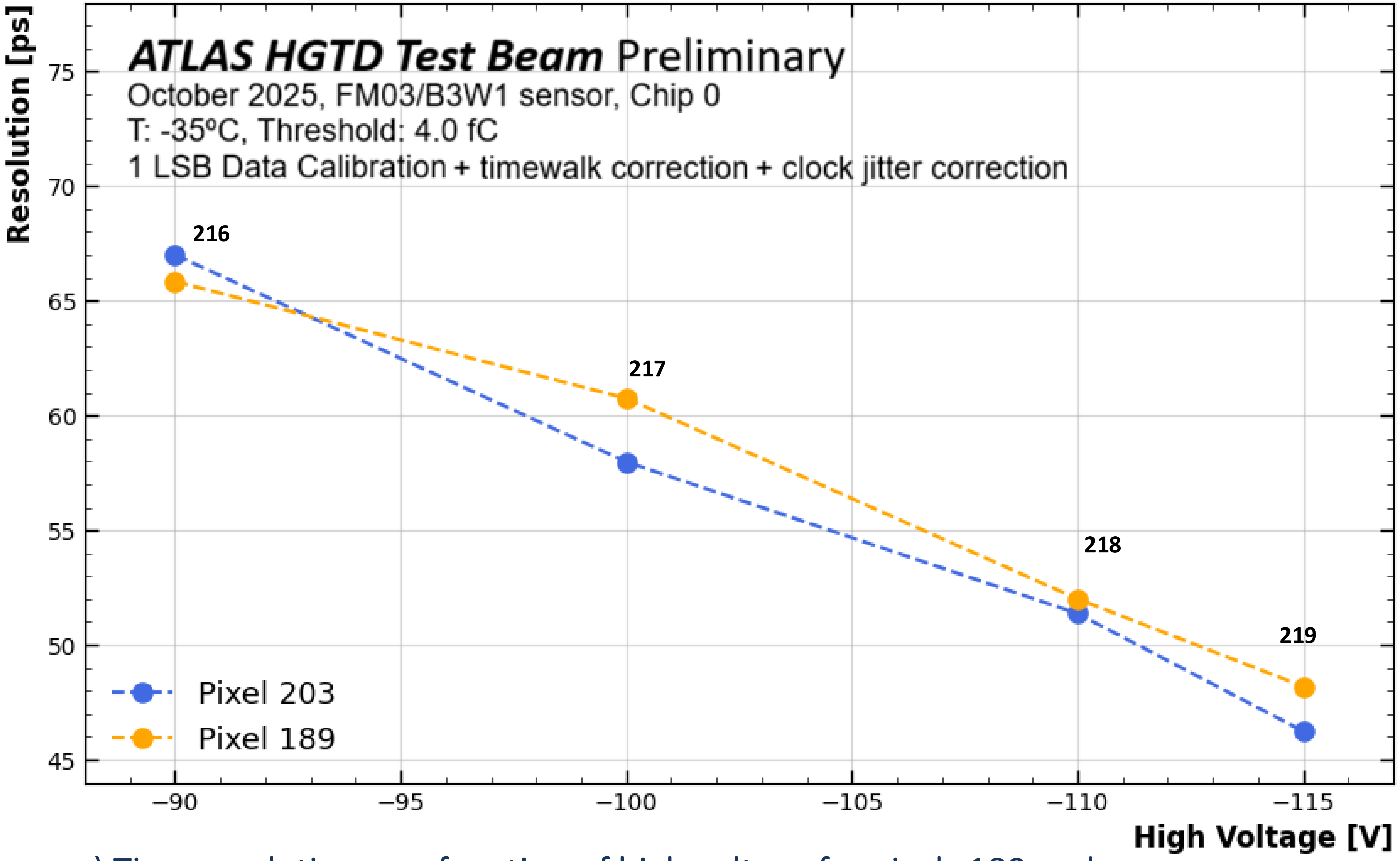


b) Residual Time Difference vs ToA

Test-beam measurements

Timing Performance

- Summarises the timing performance across batch 216-219
- Evaluate the consistency and reproducibility
- **Increasing |HV| improves the time resolution** (lower resolution values are better)
- Both pixels show **consistent behaviour**, demonstrating good reproducibility
- Best measured resolution reaches ≈**46–48 ps** at **−115V**, approaching the HGTD design target



a) Time resolution as a function of high voltage for pixels 189 and 203 (batches 216–219)

Credit: Pau Fuste Martin

Conclusions

- HGTD will **mitigate** the **pile-up effects** for the HL-LHC
  - Thanks to LGAD technology for its time resolution

- **Module assembly and testing procedure** established
  - Pre-production ongoing with more than 50 functional modules

- Full **ALTIROC-A modules tested at test beam**
  - Hit efficiency of above 98% in the gain region
  - Time resolution below 50 ps

Future work:

- Plans to continue **testing modules at future test beams**
  - Testing of irradiated modules, for the first time

Thank you

The pile-up will be caused by the increase of the instantaneous luminosity

● Pile-up <> = 200 interactions per bunch crossing, spread in ~45 mm along the beam axis.

● The **Inner Tracker (ITk)** mostly mitigates the pile-up effect but is still challenging in the forward region.

● To discriminate between pile-up and hard scattering interaction, the HGTD will be added in the forward region with the goal to have 30-50 ps per track time resolution (beginning-end).

● By utilizing both spatial and timing information, we can confidently link tracks to vertices in the forward region.

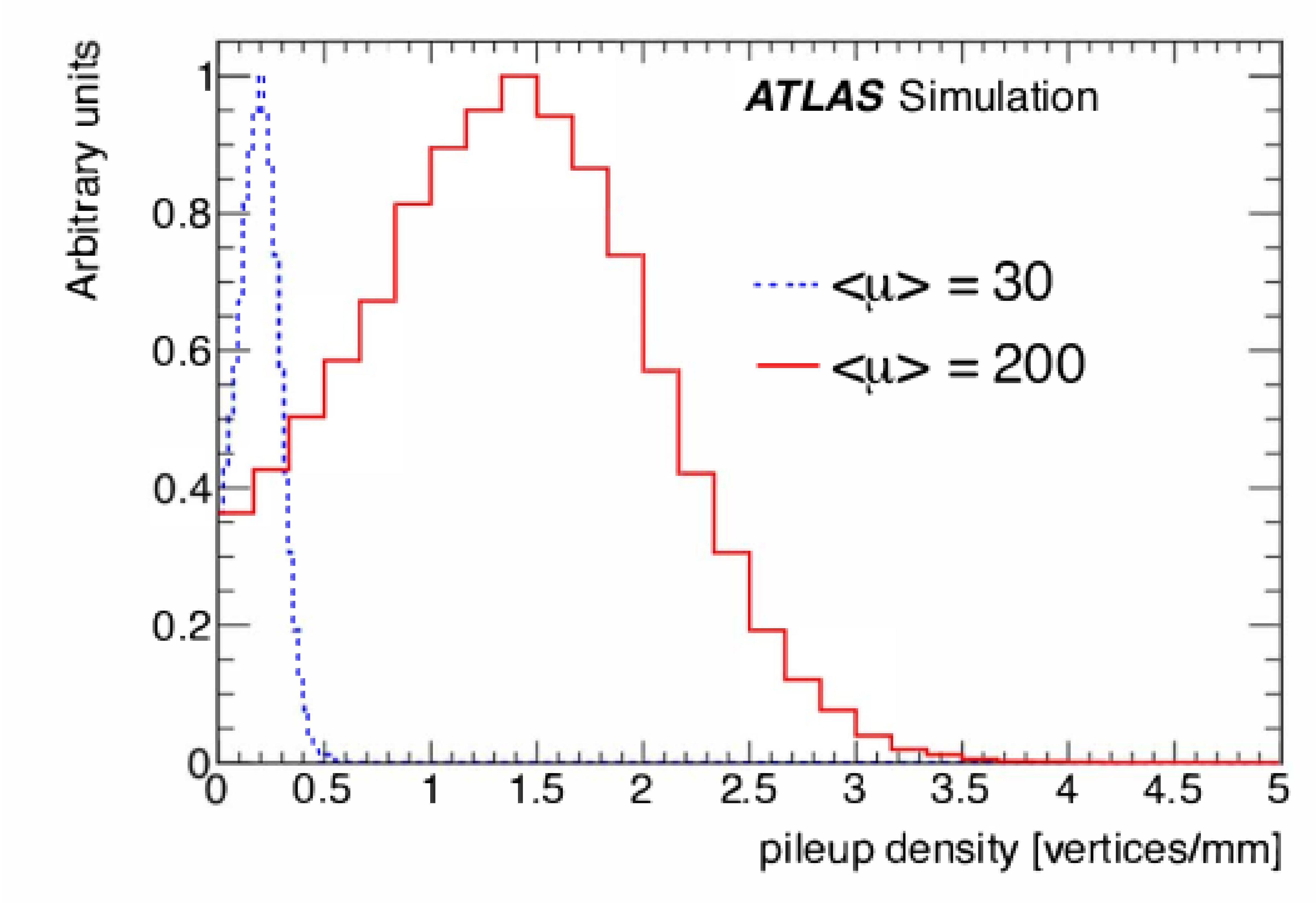


Figure: Pile-up differences