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Time to digital converter based on FPGA

This research focuses on the design and development of high-resolution Time-to-Digital Converters (TDCs) and explores key parameters for evaluating their performance. Among various time-to-digital conversion methods, three approaches are examined in detail: counter-based, delay line-based (including Vernier, buffer, and inverter-based delay lines). The study specifically investigates the implementation of a buffer delay line TDC, where inverters connected with ideally zero-delay wires serve as buffers. A counter-based TDC is used for coarse measurement, while the buffer delay line is employed for fine measurement, enabling the detection of smaller time intervals that cannot be resolved by a counter alone.

The proposed TDC architecture can be implemented on both Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs).The building blocks of the TDC circuit are simulated using Verilog HDL, and the overall TDC block diagram is presented. The simulations of both coarse and fine measurement components yield results consistent with the operating principles of a TDC, demonstrating the effectiveness of the proposed design.

Apply for student award at which level:

None

Consent on use of personal information: Abstract Submission

Yes, I ACCEPT

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